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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,975	CRUTCHFIELD ET AL.	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5 - 16, 18 - 32* is/are rejected.

7)☒ Claim(s) *4, 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

With regard to applicant's argument regarding the detection of a difference signal level change. Ryan ('946) clearly detects a signal edge change (see figure 5, 66) for an incoming data signal (see figure 5, 10). While examiner has noted applicant's argument regarding difference signal as design choice being unfounded, examiner chooses not to withdraw this rejection. While not revising grounds of rejection, examiner will introduce into evidence Grimm (US-3,609,662) as an example of the use of a differential receiver used in conjunction with a data receiver as an illustrative example that the use of a differential receiver is hardly a novel concept in the art.

With regard to claim 1 and applicant's argument of ignoring a difference signal. First, this limitation does not affect the operation of the other steps of the claim, which describe the basic operation of a counter circuit and does not appear to affect the basic operation of the counter or change its fundamental operation, and does not change examiner's rationale with respect to difference signal or ignoring signal.

With respect to applicant's argument regarding claim 2. Ryan ('946) shows a SCLK output (see figure 5, SCLK), which is derived from Bit Rate counter (see figure 5, 60) and is used to clock data (see column 9, lines 48 – 65) and therefore generates a sampling pulse as required by the claim. When considered as a whole, Ryan is interpreted as reading on applicant's invention.

With respect to applicant's argument regarding claim 3. Ryan ('946) describes this operation as either being operable as an up or down counter (see column 9, line 27 – 47). Examiner further notes that this is a basic function of a counter as taught in digital logic design and therefore does not represent a novel concept. When considered as a whole, Ryan is interpreted as reading on applicant's invention.

With respect to applicant's argument regarding claim 5. Examiner has reviewed the cited passages of Ryan ('946), and will point out that the paragraph (see column

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 9/12/2005 have been fully considered but they are not persuasive. Examiner is maintaining requirement for terminal disclaimer to be filed with respect to co-pending application 09/859782. The distinction between defining a sample count value ('782) and calculating a sample count value does not represent a patentable distinction as the setting of data rates is well known in the art as setting clock dividers / counters. Further, the different standards supported by the inventions rely on the same fundamental underpinnings, and therefore requirement for terminal disclaimer is maintained.

2. Applicant's arguments, see page 16, filed 9/12/05, with respect to details of claim 4 (and claim 17) have been fully considered and are persuasive. The rejection of claims 4 and 17 has been withdrawn.

3. Applicant's arguments filed 9/12/2005 have been fully considered but they are not persuasive.

Claims 1, 10, 19, 24, and 28 recite the limitation of generating a difference signal, which while allowing for applicant's ability to be his own lexicographer, is interpreted by examiner as reception of a differential signal and converting it to a single ended signal (see IEEE definition included as NPL for clarification). Unless there is a unique and different aspect this limitation is interpreted as describing a differential receiver, which is one of the fundamental building blocks in communications systems and therefore not unique when addressing the reception of a serial data signal.

10, lines 26 – 42) does describe the resetting of a counter upon detection of an edge (column 10, lines 29 – 39). Examiner reminds applicant that reference must be considered as a whole, and that Ryan is interpreted as reading on this limitation.

With regard to applicant's argument regarding claims 6 – 9. Ryan ('946) describes an invention for the synchronization of a clock with data (see abstract), which is a generic invention. IEEE 1394b is a specific communications specification, which could be easily applied to a generic communications adapter, and would be obvious to one of ordinary skill in the art at the time of invention.

With regard to claims 11 – 16, 18 - 19, see arguments above for claims 1 – 3, 5 – 9.

With regard to claim 19, as discussed above applicant's claim language is describing a differential receiver and as noted above does not appear to represent a novel concept in the art. Further, Ryan ('946) does describe operation of a device to extract data according to a communication link speed (see column 3, lines 10 –20; column 3; line 51 – 63) where programmable bit-rate value is fairly interpreted as a variable representative of communication link speed (see other cited prior art '407 and '837).

With respect to applicant's argument regarding claim 24. As noted above in claim 1 difference signal does not appear to constitute a novel limitation on its own. Regarding encoded data output, given that claim requires downstream use of a decoder the output of encoded data is required for decoder to operable and therefore inherent. Examiner calls applicant's attention to IEEE P1394b, Draft 1. 11, figures 4-1 and 10-2, which discloses the set of elements claimed by applicant. Examiner also points out to applicant that the disclosure of IEEE 1394b standard makes 1394b acknowledged as prior art to applicant.

With regard to claim 28, and applicant's amendment and arguments. Examiner will maintain the rejection of claim 28 using Ryan ('946) with the additional explanation. Ryan in figure 3 discloses an OSC signal ,which is described as a high speed clock (see column 8, lines 26 – 35). This is important as careful reading as Ryan as a whole describes a digital synchronous logic design where high speed clock is used to align edges of signals. In particular, Ryan discloses the alignment of sampling clock (SCLK) to a master clock phase (see column 10, lines 26 – 42) where it is clear that a higher speed clock is used to control the output of sampling clock.

4. Restatement / clarification (claims 24 & 25) of previous rejections.

Claims 1 – 3, 5 – 16, 18, 19, and 22 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US 6,359,946).

With regard to claim 1, Ryan discloses a method for effecting synchronous pulse generation for use in variable speed serial communications, comprising the steps of: obtaining a communication link speed (see column 9, lines 38 – 47 where this is interpreted as equivalent); providing a clock signal (see column 9, lines 27 – 30), providing a counter (see figure 5, 60 and column 9, lines 24 – 30), defining a sample count value of counter using communication link speed (see column 9, lines 30 – 33 where this is interpreted as equivalent), incrementing counter in relation to clock signal, determining whether current count value of counter corresponds to sample count value, and if current count value corresponds to sample count value then performing a step of generating a synchronous pulse (see column 9, lines 33 – 41), and if current count value does not correspond to sample count value then performing a step of determining whether a signal level has changed, and if difference signal has changed then performing a step of ignoring further changes in signal level of difference signal until current count value of counter corresponds to sample count value at which time step of generating synchronous pulse is repeated (see column 9, line 66 – column 10, line 8). Ryan is silent with respect to "difference signal." Ryan does teach a method of receiving serial

communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 2, Ryan teaches a method wherein synchronous pulse is used to signify a time for performing a step of sampling difference signal to extract data from difference signal (see figure 1, SCLK, data signal, 200 and column 13, lines 22 – 25).

With regard to claim 3, Ryan teaches a method further comprising a step of defining a maximum count value of counter wherein if current count value corresponds to maximum count value then performing a step of resetting counter (see column 9, lines 33 – 41).

With regard to claim 5, Ryan teaches a method wherein step of ignoring further changes in signal level of difference signal further comprises the steps of: resetting counter (see column 10, lines 26 – 29), determining whether current count value corresponds to sample count value; and if current count value does not correspond to sample count value the performing step of incrementing counter each clock cycle until current count value corresponds to sample count value at which time a step of sampling difference signal to extract data from difference signal is performed (see column 9, lines 33 – 41).

With regard to claim 6 - 9, Ryan is silent with respect to IEEE – 1394b communications link speeds. Ryan teaches a serial communications receiver capable of various data rates and types (see column 9, lines 41 – 47). IEEE – 1394b is a known serial communications data standard and therefore would have been obvious to one of ordinary art to adapt Ryan's serial communications receiver to support communication link speeds as defined in IEEE – 1394b communications standards.

With regard to claim 10, Ryan discloses a method of extracting data, comprising the steps of: providing a clock signal (see column 9, lines 27 – 30), determining a communication link speed (see column 4, lines 48 – 52 where this is interpreted as equivalent); providing a counter (see figure 5, 60 and column 9, lines 24 – 30), defining a sample count value of counter utilizing communication link speed (see column 9, lines 30 – 33), incrementing counter in relation to clock signal, determining whether current count value of counter corresponds to sample count value, and if current count value corresponds to sample count value then

performing a step of generating a synchronous pulse (see column 9, lines 33 – 41), and if current count value does not correspond to sample count value then performing a step of determining whether a signal level has changed, and if difference signal has changed then performing a step of ignoring further changes in signal level of difference signal until current count value of counter corresponds to sample count value at which time step of generating synchronous pulse is repeated (see column 9, line 66 – column 10, line 8). Ryan is silent with respect to "difference signal." Ryan does teach a method of receiving serial communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 11, Ryan teaches a method wherein current count value corresponds to sample count value, method further comprises step of generating a synchronization pulse to signify a time for sampling of difference signal to extract data from difference signal (see figure 5, SCLK, data signal, 200 and abstract).

With regard to claims 12 – 16 and 18, these claims are analyzed as claims 6 – 9, 3 and 5, respectively, above.

With regard to claim 19, Ryan teaches a variable speed communications device comprising; a synchronous pulse generator having a data signal input (see figure 5, data signal), a clock signal (see column 9, lines 27 – 30), a speed input (see column 9, lines 30 – 33 where this is interpreted as equivalent), and a synchronous pulse output (see figure 5, SCLK where this is interpreted as equivalent), speed input adapted to receive a variable representative of a communications link speed (see column 9, lines 30 – 33) and a data signal input being coupled to receive data signal and clock signal input adapted to receive a clock signal (see column 9, lines 27 – 30 where this is interpreted as equivalent), wherein synchronous pulse generator processes clock signal and data signal to generate as synchronous pulse used for extracting data using clock signal (see figure 5, and column 9, lines 27 – 33 where this is interpreted as equivalent), and sampling data signal when synchronous pulse is asserted (see column 13, lines23 – 26 where SCLK is interpreted as clocking signal output as a synchronous pulse). Ryan is silent with respect to "difference

signal." Ryan does teach a method of receiving serial communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 22 and 23, Ryan teaches an apparatus wherein synchronous pulse generator comprises means for selecting between data rates (see column 9, lines 41 – 47 where this is interpreted as equivalent functionality). Ryan is silent with respect to IEEE-1394 communication bus speeds. Ryan teaches a serial communications receiver capable of various data rates (see column 9, lines 41 – 47). IEEE-1394 is a known serial communications data standard and therefore would have been obvious to one of ordinary art to adapt Ryan's serial communications receiver to support IEEE-1394 standards.

With regard to claim 24, Ryan teaches a communications device comprising; a synchronous pulse generator having a data signal input (see figure 5, data signal), a clock signal (see column 9, lines 27 – 30), a speed input (see column 9, lines 30 – 33 where this is interpreted as equivalent), and a synchronous pulse output (see figure 5, SCLK where this is interpreted as equivalent), speed input adapted to receive a variable representative of a communications link speed (see column 9, lines 30 – 33) and a data signal input being coupled to receive data signal and clock signal input adapted to receive a clock signal (see column 9, lines 27 – 30 where this is interpreted as equivalent), wherein synchronous pulse generator processes clock signal and data signal to generate as synchronous pulse used for extracting data using clock signal (see figure 5, and column 9, lines 27 – 33 where this is interpreted as equivalent), and sampling data signal when synchronous pulse is asserted (see column 13, lines23 – 26 where SCLK is interpreted as clocking signal output as a synchronous pulse), a serial interface engine having a 2nd difference signal input, a synchronous pulse input, and a parallel output, and SIE processing serial data and outputting parallel data (see figure 5, 200, data signal, SCLK; figure 7, and column 13,

lines 23 – 39 where this is interpreted as equivalent functionality). . Ryan is silent with respect to "difference signal", IEEE-1394b, 8b/10b decoder, and descrambler. Ryan discloses a method of receiving serial communications of which IEEE-1394b is a known standard utilizing differential signals for the transmission of serial data and therefore would have been obvious for an IEEE-1394b system application. Applicant's disclosure (figure 10) of IEEE 1394b communications device clearly defines the requirements for an 8b/10b decoder and descrambler (see also, for example IEEE 1394b, Draft 1.11, figure 10-2 and last paragraph of page 141). It would have been obvious to one of ordinary skill in the art at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42).

With regard to claim 25, Ryan is silent on the use of connection manager having a toning input, a toning output and a bus speed output. Applicant's discloses use of IEEE 1394b standard, which defines the use of connection manager having a toning input, a toning output and a bus speed output (see, for example, IEEE 1394b, Draft 1.11, section 6.6, 6,6,1). It would have been obvious to one of ordinary skill in the art at the time of invention to support an IEEE 1394b system in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42).

With regard to claims 26– 27, these claims are analyzed as claims 22 and 23 above.

With regard to claim 28, Ryan discloses a method for synchronizing a receiver to data, comprising the steps of: detecting a data speed (see column 4, lines 48 – 52), initializing a counter to count clock cycles (see column 9, lines 30 – 33 where loading of bit-rate value is interpreted as performing this function), detecting a current counter value (see column 9, lines 33 – 41), defining a sampling count value based on data speed (see figure 5, 60 and column 9, lines 24 – 30), detecting a change in data (see figure 3, edge), incrementing counter if no

change in data is detected, generating a synchronous pulse when counter reaches sampling count value (see column 9, lines 33 – 41). Ryan is silent with sampling data with clock when pulse is asserted. Ryan does teach that SCLK (synchronous pulse) is derived from single clock. Using a combinatorial logic function of SCLK and system clock would be a design choice.

With regard to claim 29, Ryan teaches a method wherein generating step occurs if a change in data is detected (see column 10, lines 13 – 18).

With regard to claim 30, Ryan teaches a method wherein generating step occurs when count value equals sampling count value (see column 9, lines 33 – 41).

With regard to claim 31, Ryan teaches a method further comprising the step of delaying pulse to center pulse in a data bit (see column 11, lines 17 – 21 where this is interpreted as inclusive).

With regard to claim 32, Ryan teaches a counter where this is an inherent feature of a modulo-n counter.

Claims 20 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US 6,359,946) in view of IEEE-1394b, Draft 1.11.

With regard to claim 20, Ryan teaches a variable speed communications device further comprising a comprising a serial interface engine having a 2nd difference signal input, a synchronous pulse input, and a parallel output, and SIE processing serial data and outputting parallel data (see figure 5, 200, data signal, SCLK; figure 7, and column 13, lines 23 – 39 where this is interpreted as equivalent functionality). Ryan is silent with respect 8b/10b decoder, and descrambler. IEEE-1394b, figure 10-2 clearly defines the requirements for an 8b/10b encoder and scrambler along with the needs for reciprocal functions (page 141 last paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable

for various communications standards (see column 2, lines 37 – 42). The particular circuit naming convention as claimed by applicant is design choice.

With regard to claim 21, Ryan is silent with respect to a packet receiver / transmitter having a parallel input, parallel input coupled to parallel output of descrambler. IEEE-1394b, figure 4-1 clearly shows a packet receiver/transmitter, which connects to communication port incorporating other limitations. It would have been obvious to one of ordinary skill in the art at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42).

Allowable Subject Matter

5. Claims 4 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1 – 5, 10, 11, 16 – 19, 28 - 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1- 5, 9, 10, 14 – 17, 27 – 31, respectively, of copending Application No. 09/895782 in view of the identical recitations of the claims. Examiner notes that there a subtle variations in the claims but believes that the differences are synonymous with the definitions of the original claims.

This is a provisional obviousness-type double patenting rejection.

Other Cited Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Grimm (US-3,609,662) discloses the use of a differential receiver in conjunction with a data receiver.

Chun et al (US-4,280,221) discloses the use of a differential receiver in conjunction with a data receiver.

Hofsaess (US-5,696,777) discloses the use of a differential receiver in conjunction with a data receiver.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM
11/23/05

TEMESGHEN GNEBRETINSAE
PRIMARY EXAMINER
11/28/05